

### REMARKS

Claims 2-7, 9-13, 15-18, 20-25, 27-30, and 32-39 are pending in the present application. In the office action mailed June 5, 2003 ("the Office Action"), the Examiner indicated that claims 2-39 were pending in the present application, and that claims 1, 8, 14, 19, 26, and 31 had been withdrawn from consideration. However, claims 1, 8, 14, 19, 26, and 31 were previously *cancelled* by amendment (and not simply withdrawn from consideration). Thus, as previously mentioned, only claims 2-7, 9-13, 15-18, 20-25, 27-30, and 32-39 are currently pending.

In the Office action, claim 30 was rejected under 35 U.S.C. 112, second paragraph, for indefiniteness because of insufficient antecedent basis. Claims 2-7, 9-13, 15-18, and 32-39 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,357,621 to Cox ("the Cox patent") in view of U.S. Patent No. 5,129,069 to Helm *et al.* ("the Helm patent"). Claims 20-25 and 27-30 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,252,612 to Jeddeloh ("the Jeddeloh patent") in view of the Cox patent, and further in view of the Helm patent.

With respect to the rejection of claim 30, claim 30 has been amended to correct its claim dependency from claim 26, which had been previously cancelled, to claim 28. Similarly, claim 18 has been amended to depend from claim 16, rather than previously cancelled claim 14.

Claim 22 has also been amended to correct a typographical error. It will be appreciated that the amendments described herein are not substantially related to patentability, and should not be interpreted as narrowing amendments.

As previously mentioned, claims 2-7, 9-13, 15-18, and 32-39 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Cox patent in view of the Helm patent.

The Examiner argues that the Cox patent teaches "all the limitations of claims 4, 10, 16, except for that the memory module controllers do not directly access memory requests," however, the Helm patent teaches a memory apparatus for a computer which includes "memory module[s that] can access memory requests from the CPU 11." See the Office Action at pp. 3 and 4. The Examiner further argues that "it would have been obvious to one skilled in the art to utilize the memory system as taught by [the Helm patent] in combination with the memory

system as taught by [the Cox patent] in order to provide an automatic memory configuration in a manner which is highly efficient and yet involves minimal hardware cost.” *Id.*

Applicants disagree with the Examiner’s characterization of both the Cox patent and the Helm patent. Moreover, even if it is assumed that the Examiner’s characterization of the Cox and Helm patents are correct, the limitation on which the Examiner is focusing is not one recited in claims 4, 10, 16, 35 or 37.

As discussed in a previously submitted response to office action, the Cox patent describes an expandable memory system for a serial network. The memory system includes a central memory system controller and individually addressable memory module controllers serially coupled to the memory system controller through a “memory control link” (MCL). An advantage provided by the expandable memory system, or “MCL system” (Figure 1), described in the Cox patent is that the total capacity of the memory system can be increased or changed by plugging in or removing memory module cards, and the memory system automatically assigns the addresses and memory block positions of the modules in the total memory space without user intervention or the need to physically reposition toggle or slide switches. This is accomplished through the use of the memory system controller communicating with the memory module controller of each memory module via the MCL.

As described in the Cox patent, “the MCL system 10 is used only to interrogate and configure the memory modules 20, and is not used during real time memory accesses by the host system.” Col. 4, lines 62-65. The interrogation and configuration process occurs only at start-up, at which time, the memory system controller interrogates the memory modules (*i.e.*, the memory module controller for each memory module) for its memory size and type and assigns a starting address for each of the memory modules. *See* col. 5, lines 3-44. After the interrogation and configuration process is completed, the memory system operates in a conventional manner with little interaction by the MCL controllers 22. That is, memory access commands and data are transferred to and from the memory devices in the conventional manner.

As shown in Figure 2, each of the memory blocks 23, 25, 27, and 29 are coupled to a data bus 32, an address bus 28, and a RAS signal line 26 so that each of the memory blocks can be accessed accordingly by the system DRAM controller. A CAS signal line 37A is provided to a memory block control logic 21 for the selection of which memory block 23, 25, 27,

or 29 will be activated. The selection of which memory block is based on the address assigned to the memory module 20 by the memory system controller 11. As further shown in Figures 1 and 2, the MCL system 10, that is, the memory system controller, the MCL, and the memory module controller of each memory module, is provided for the limited purpose of memory space allocation. None of the elements have access to data stored by the addressable memory address space, nor do they receive memory access requests. For example, the MCL, which essentially consists of control lines 18a-c, and reset line 16, is limited to serial communication of configuration data from the system controller 11 to the MCL controller 22 of each memory module 20. The MCL is not designed to transfer memory access requests or data. Moreover, the data bus 32 and the MCL controller are not coupled in any manner, which clearly indicates that the MCL controllers never handle any data during a memory access operation.

Thus, despite the Examiner's statement that the Cox patent describes all of the limitations of claims 4, 10, and 16 except for the memory module controllers directly accessing memory requests is not correct. The Cox patent fails to describe at least the first and second memory controllers that receive memory requests. The Cox patent further fails to teach a memory controller bus coupled between the first and second memory controllers on which memory access requests can be passed.

The Helm patent similarly describes a memory apparatus for a computer which can automatically effect memory configuration of a system memory. Figure 1 illustrates the computer system 10 in which the memory apparatus is implemented for automatic memory configuration. Figure 2 illustrates a memory expansion board 24 that can be inserted into the computer system 10 through board slots 17-19. As described in the Helm patent, automatic memory configuration is accomplished by performing the program shown in Figure 3 and storing basic memory configuration information for the respective memory expansion board 24. As with the Cox patent, the configuration program described in the Helm patent is performed at the time the computer system 10 is powered up. Contrary to the Examiner's characterization, however, although each memory module receives memory access requests from the CPU 11, the memory address decoding section 32 does not ever receive any of the memory access requests. Moreover, the address decoding section 32 does not have any access to the data stored by the addressable memory space. These deficiencies are evident in Figure 2 of the Helm patent, and

the description found at col. 4, line 20-col. 6, line 52. As shown in Figure 2, the memory control signals 16 are provided directly to the memory storage section 31, and completely bypass the memory address decoding section 32. Moreover, as further shown in Figure 2, the data stored by the memory storage section 31 is not provided in any way to the memory address decoding section 32. The only connection between the memory address decoding section 32 and the data bus is for the CPU to provide configuration information to the configuration register 36. However, data stored by the memory storage section 31 does not pass through the memory address decoding section 32. Thus, the Examiner's characterization that Helm teaches a memory module controller that accesses memory requests in inaccurate based on material found within the Helm patent itself.

Claim 4 is patentable over the Cox patent in view of the Helm patent because the combined teachings of the patents fail to teach or suggest the combination of limitations recited by claim 4. For example, and as previously discussed, the Cox and Helm patents fail to teach a first memory controller receiving memory access requests to a block of memory to which a functional memory sub-array from the first memory array is assigned in combination with first and second memory controllers coupled together by a memory controller bus on which memory access requests received by one of the memory controllers can be passed to the other memory controller in order to access a memory location in the memory array coupled to that memory controller. The Cox patent merely describes a memory system having MCL controllers of each module coupled in a serial fashion for the limited purpose of allocating a total memory space. None of the MCL controllers handle memory access requests or data, or forwards the same to another MCL controller. The memory banks are coupled directly to common command, address, and data busses over which memory access requests are received by the memory banks directly from the DRAM controller 33. Similarly, the Helm patent teaches a memory expansion board 24 that includes a memory address decoding section 32 that is used in automatically configuring the memory system. Despite the Examiner's belief to the otherwise, the memory address decoding section neither receives memory access requests, or has access to the data stored by the memory storage section. For the foregoing reasons, claim 4 is patentable over the Cox patent in view of the Helm patent, and therefore, the rejection of claim 4 under 35 U.S.C. 103(a) should be withdrawn.

Claims 10 and 16 are also similarly patentable over the Cox patent in view of the Helm patent because the combined teachings of the Cox and Helm patent fail to teach or suggest the combination of limitations recited by either claims 10 or 16. For example, as previously discussed with respect to claim 4, the Cox and Helm patents do not describe a memory system having the memory controllers coupled to the respective registers to consult pointer values to determine the functional memory sub-arrays in combination with a memory controller bus coupling the memory controllers over which memory access requests received by one of the memory controllers can be passed to the other memory controller. For the foregoing reasons, claims 10 and 16 are patentable over the Cox patent in view of the Helm patent. Therefore, the rejection of claims 10 and 16 under 35 U.S.C. 103(a) should be withdrawn.

Claim 35 and 37 are also patentable over the Cox patent in view of the Helm patent. The Cox and Helm patents fail to teach or suggest the combination of limitations recited by claims 35 and 37. For example, as previously discussed with claims 4, 10, and 16, neither the Cox or Helm patents teach or suggest the combination of assigning each functional memory sub-array of the memory array to a respective memory block and leaving any faulty memory sub-arrays unassigned, determining from the start address and size values whether the particular memory block of the memory access request is assigned to a memory sub-array within the addressable memory area of the memory array, and servicing the memory access request if the particular memory block is determined to be assigned to a memory sub-array within the addressable memory area of the memory array, or otherwise passing the memory access request to another memory controller for servicing. For the foregoing reasons, claims 35 and 37 are patentable over the Cox patent in view of the Helm patent, and the rejection of claims 35 and 37 under 35 U.S.C. 103(a) should be withdrawn.

Claims 2, 3, and 5-7, which depend from claim 4, claims 9 and 11-13, which depend from claim 10, claims 15, 17, and 18, which depend from claim 16, claims 32-34, and 36, which depend from claim 35, claims 38 and 39, which depend from claim 37, are similarly patentable over the Cox patent in view of the Helm patent based on their dependency from an respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. However, because each claim in an

application represents a different invention, the rejection of an independent claim does not necessarily result in the rejection of claims depending therefrom. For the foregoing reasons, the rejection of claims 2, 3, 5-7, 9, 11-13, 15, 17, 18, 32-34, 36, 38, and 39 under 35 U.S.C. 103(a) should be withdrawn.

As previously mentioned, claims 20-25 and 27-30 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Jeddelloh patent in view of the Cox patent, and further in view of the Helm patent. Claims 22 and 28 are patentable over the Jeddelloh patent in view of the Cox patent, and further in view of the Helm patent because the combined teachings of the references do not teach or suggest the combination of limitations recited by claims 22 and 28.

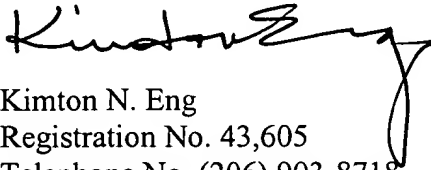
The Examiner has cited the Jeddelloh patent as teaching all of the limitations of claims 22 and 28 except that “the first memory and the second memory are segmented into plurality of memory sub-arrays, and the first memory controller and the second memory controller coupled to the memory request to receive memory access requests.” *See* the Office Action at pp. 6 and 7. Without addressing the merits of the Examiner’s characterization of the teachings of the Jeddelloh patent, even if it is assumed that the Jeddelloh patent does teach the material as stated by the Examiner, those teachings do not make up for the deficiencies of the Cox and Helm patents. As previously discussed with respect to claims 4, 10, 16, 35, and 37, the Cox and Helm patents do not teach the combination of memory controllers, memory arrays, and memory controller bus as claimed in claims 22 and 28. The teachings of the Jeddelloh patent, as characterized by the Examiner, do not make up for the deficiencies in the teachings of the Cox and Helm patents.

For the foregoing reasons, claims 22 and 28 are patentable over the Jeddelloh patent in view of the Cox patent, further in view of the Helm patent. Claims 20, 21, and 23-25, which depend from claim 22, and claims 27, 29, and 30, which depend from claim 28 are also patentable based on their dependency from an allowable base claim. Therefore, the rejection of claims 20-25 and 27-30 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims remaining in the application are now clearly allowable.  
Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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